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(54) **Hermetic protection for integrated circuits, based on a ceramic layer.**

(57) This invention relates to integrated circuits which are protected from the environment. Such circuits are hermetically sealed by applying ceramic layers to the top metallization.

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The present invention relates to integrated circuits which are protected from the environment. Such circuits are hermetically sealed by applying ceramic layers to the top metallization. These circuits are inexpensive to fabricate and have improved performance and reliability.

Modern electronic circuits must be able to withstand a wide variety of environmental conditions such as moisture, ions, heat and abrasion. A significant amount of work has been directed toward various protective measures to minimize the exposure of such circuits to the above conditions and thereby increase their reliability and life.

Many prior art processes for protecting electronic circuits involve sealing or encapsulating the circuits after they have been interconnected. For example, it is known in the art to use protective layers of silicones, polyimides, epoxies, other organics, plastics and the like. Such materials, however, are of only limited value since most are permeable to environmental moisture and ions.

Similarly, interconnected circuits have also been sealed within ceramic packages. This latter approach has proven to be relatively effective in increasing device reliability and is currently used in select applications. The added size, weight and cost involved in this approach, however, inhibits widespread application in the electronic industry.

The use of lightweight ceramic protective coatings on electronic devices has also been suggested in U.S. Patents 4,756,977 and 4,749,631. The use of ceramic silica coatings are described therein which are derived from hydrogen silsesquioxane and silicate esters, respectively, as well as the use of additional ceramic layers as hermetic barriers. We have discovered that when such coatings are applied specifically to integrated circuits at the wafer stage and, even though the bond pads are subsequently opened by removing a portion of the coating, the resultant circuits remain hermetically sealed and exhibit increased reliability and life.

Sealing circuits at the wafer stage is also known in the art. For example, it is known in the art to coat fabricated integrated circuits with ceramic materials such as silica and/or silicon nitride by chemical vapor deposition (CVD) techniques. These coatings are then etched back to the bond pads for the application of leads. The wafers coated in this manner, however, have inadequate reliability and life.

We have found a solution to the above problems associated with the hermetic protection of integrated circuits by replacing the conventional passivation layers on integrated circuits with the silicon-containing ceramic coatings described herein.

The present invention relates to hermetically sealed integrated circuits. These circuits comprise circuit subassemblies having a top layer of metallization including one or more bond pads. To this top layer of metallization is applied a silicon-containing ceramic layer by a process comprising coating the circuit with a composition comprising a preceramic silicon-containing material followed by converting said material to a ceramic. The ceramic layers covering the bond pads may optionally be removed and the resultant open bond pads sealed with one or more non-corroding, conductive layers.

The present invention also relates to a method for producing the above sealed integrated circuits. The method involves applying one or more ceramic layers over the top layer of metallization on the circuit followed by removing at least a portion of the ceramic layer covering the bond pads.

The present invention is based on our finding that integrated circuits can be hermetically sealed by the application of the ceramic coatings taught herein over the top layer of metallization on the circuit. These sealed circuits have increased reliability and performance. In addition, since this process is unexpectedly performed at the wafer stage, production can be simplified and costs reduced.

The integrated circuit subassemblies used in the process of this invention are not critical and nearly any which are known in the art and/or produced commercially are useful herein. The processes used to produce such circuits are also known and not critical to the invention. Exemplary of such circuits are those comprising a semiconductor substrate, such as silicon or gallium arsenide, having an epitaxial layer grown thereon. This epitaxial layer is appropriately doped to form the PN-junction regions which constitute the active regions of the device. These active regions are diodes and transistors which form the integrated circuit when appropriately interconnected by a properly patterned metallic layer. This metallic interconnect layer terminates at the bond pads on the exterior surface of the circuit subassembly.

As described above, the prior art discloses passivating such circuits with one or more ceramic coatings applied by CVD techniques. These coatings included, for example, silica, silicon nitride or silicon oxynitride derived from precursors such as silane and oxygen, nitrous oxide, nitrogen, ammonia or the like. Circuits coated with such a passivation layer, however, are still prone to damage by the environment. For example, the passivation is prone to penetration of water and/or various destructive ions through defects and cracks. As noted above, the circuit industry has attempted to solve these problems by the use of additional protective measures after the circuits are interconnected. The present invention, on the other hand, describes the application of specific ceramic coatings before the interconnection.

In the process of the present invention, the above circuits are sealed by covering the circuit's top metallization with one or more ceramic layers. The first layer is generally a silicon-containing ceramic material

which is applied by a process comprising coating the circuit with a composition comprising a preceramic silicon-containing material followed by converting the preceramic silicon-containing material to a ceramic. Typically, the preceramic material is converted to a ceramic by heating it to a sufficient temperature.

As used in the present invention, the term "preceramic silicon-containing material" describes material which can be rendered sufficiently flowable to impregnate and coat the surface of a circuit and which can be subsequently converted to a solid layer exhibiting properties generally recognized by those skilled in the art as characteristic of a ceramic. These materials include, for example, precursors to silicon oxides, silicon nitride, silicon oxynitride, silicon oxycarbide, silicon carbonitride, silicon oxycarbonitride, silicon carbide and the like.

The preferred preceramic compounds to be used in the process of this invention are precursors to silicon oxides, especially silica. The silica precursors which may be used in the invention include hydrogen silsesquioxane resin (H-resin), hydrolyzed or partially hydrolyzed $R_nSi(OR)_{4-n}$, or their combinations, in which each R is independently an aliphatic, alicyclic or aromatic substituent of 1-20 carbon atoms, preferably 1-4 carbon atoms, such as an alkyl (e.g., methyl, ethyl, propyl), alkenyl (e.g., vinyl or allyl), alkynyl (e.g., ethynyl), cyclopentyl, cyclohexyl and phenyl and n is 0-3, preferably 0-1.

H-resin is used in this invention to describe a variety of hydridosilane resins having units of the structure $HSi(OH)_x(OR)_yO_{z/2}$ in which each R is independently an organic group which, when bonded to silicon through the oxygen atom, forms a hydrolyzable substituent, x = 0-2, y = 0-2, z = 1-3 and $x + y + z = 3$. These resins may be either fully condensed ($x = 0$, $y = 0$ and $z = 3$) or they may be only partially hydrolyzed (y is not 0 over all the units of the polymer) and/or partially condensed (x is not 0 over all the units of the polymer). Although not represented by this structure, various units of these resins may have either zero or more than one Si-H bond due to various factors involved in their formation and handling. Exemplary of substantially condensed (less than about 300 ppm silanol) H-resins are those formed by the process in U.S. Patent 3,615,272. This polymeric material has units of the formula $(HSiO_{3/2})_n$ in which n is generally 8-1000. The preferred resin has a number average molecular weight of from 800-2900 and a weight average molecular weight of between 8000-28,000 (obtained by gel permeation chromatography (GPC) analysis using polydimethylsiloxane as a calibration standard). When heated sufficiently, this material yields a ceramic coating essentially free of SiH bonds.

Exemplary H-resins which may not be fully condensed include those described in U.S. Patent 5,010,159 or U.S. Patent 4,999,397. Exemplary H-resins which are not fully hydrolyzed or condensed are formed by a process which comprises hydrolyzing a hydrocarbonoxy hydridosilane with water in an acidified oxygen-containing polar organic solvent.

A platinum, rhodium or copper catalyst may also be admixed with the hydrogen silsesquioxane to increase the rate and extent of its conversion to silica. Any platinum, rhodium or copper compound or complex that can be solubilized with the catalyst will be operable. For instance, an organo-platinum composition such as platinum acetylacetonate or rhodium catalyst $RhCl_3[S(CH_2CH_2CH_2CH_3)_2]_3$, Dow Corning Corporation, Midland, Michigan are all within the scope of this invention. The above catalysts are generally added to the solution in an amount of between about 5 and 500 ppm platinum or rhodium based on the weight of resin.

The second type of silica precursor material useful herein includes hydrolyzed or partially hydrolyzed compounds of the formula $R_nSi(OR)_{4-n}$ in which R and n are as defined above. Some of these materials are commercially available, for example, under the tradename ACCUGLASS. Specific compounds of this type include methyltriethoxysilane, phenyltriethoxysilane, diethyldiethoxysilane, methyltrimethoxysilane, dimethyldimethoxysilane, phenyltrimethoxysilane, vinyltrimethoxysilane, tetramethoxysilane, tetraethoxysilane, tetrapropoxysilane and tetrabutoxysilane. After hydrolysis or partial hydrolysis of these compounds, the silicon atoms therein may be bonded to C, OH or OR groups, but a substantial portion of the material is believed to be condensed in the form of soluble Si-O-Si resins. Compounds in which $x = 2$ or 3 are generally not used alone as volatile cyclic structures are generated during pyrolysis, but small amounts of said compounds may be cohydrolyzed with other silanes to prepare useful preceramic materials.

In addition to the above SiO_2 precursors, other ceramic oxide precursors may also be advantageously used herein either solely or in combination with the above SiO_2 precursors. The ceramic oxide precursors specifically contemplated herein include compounds of various metals such as aluminum, titanium, zirconium, tantalum, niobium and/or vanadium as well as various non-metallic compounds such as those of boron or phosphorous which may be dissolved in solution, hydrolyzed and subsequently pyrolyzed at relatively low temperatures to form ceramic oxides.

The above ceramic oxide precursor compounds generally have one or more hydrolyzable groups bonded to the above metal or non-metal, depending on the valence of the metal. The number of hydrolyzable groups to be included in these compounds is not critical as long as the compound is soluble in the solvent. Likewise, selection of the exact hydrolyzable substituent is not critical since these substituents are either hydrolyzed or pyrolyzed out of the system. Typical hydrolyzable groups include alkoxy, such as me-

thoxy, propoxy, butoxy and hexoxy; acyloxy, such as acetoxy, other organic groups bonded to said metal or non-metal through an oxygen atom such as acetylacetonate or amino groups. Specific compounds, therefore, include zirconium tetracetylacetonate, titanium dibutoxy diacetylacetonate, aluminum triacetylacetonate, tetraisobutoxy titanium and $Ti(N(CH_3)_2)_4$.

When SiO_2 is to be combined with one of the above ceramic oxide precursors, generally it is used in an amount such that the final ceramic contains 70 to 99.9 percent by weight SiO_2.

Examples of suitable silicon carbonitride precursors include hydridopolysilazane (HPZ) resin and methylpolydisilylazane (MPDZ) resin. Processes for the production of these materials are described in US Patents 4,540,803 and 4,340,619. Examples of silicon carbide precursors include polycarbosilanes and examples of silicon nitride precursors include polysilazanes. Oxygen can be incorporated into the ceramics resulting from the above precursors by pyrolyzing them in an oxygen-containing environment.

The above preceramic material is then used to coat the integrated circuit. The material can be used in any practical form but it is preferred to use a solution comprising the preceramic material in a suitable solvent. If this solution approach is used, the preceramic solution is generally formed by simply dissolving or suspending the preceramic material in a solvent or mixture of solvents. Various facilitating measures such as stirring and/or heat may be used to assist in the dissolution. The solvents which may be used in this method include alcohols such as ethyl or isopropyl; aromatic hydrocarbons such as benzene or toluene; alkanes such as n-heptane or dodecane; ketones; cyclic dimethylpolysiloxanes; esters and glycol ethers, in an amount sufficient to dissolve the above materials to low solids. For instance, enough of the solvent should be included to form a 0.1-85 weight percent solution.

The circuit is then coated with this solution by means such as spin, spray, dip or flow coating and the solvent is allowed to evaporate. Any suitable means of evaporation such as simple air drying by exposure to the ambient environment, heating or the application of a vacuum may be used.

Although the above described methods primarily focus on using a solution approach, one skilled in the art would recognize that other equivalent means (eg., melt impregnation) would also function in the process of this invention.

The preceramic material is then typically converted to a silicon-containing ceramic by heating it to a sufficient temperature. Generally, the temperature is in the range of 50 to 800°C. depending on the pyrolysis atmosphere and the preceramic compound. Preferred temperatures are in the range of 50 to 600°C. and more preferably are 50-400°C. Heating is generally conducted for a time sufficient to ceramify, generally up to 6 hours, with less than 2 hours being preferred.

The above heating may be conducted at any effective atmospheric pressure from vacuum to superatmospheric and under any effective oxidizing or non-oxidizing gaseous environment such as those comprising air, O_2, an inert gas (N_2, etc.), ammonia, amines, moisture, N_2O and the like.

Any method of heating such as the use of a convection oven, rapid thermal processing, hot plate or radiant or microwave energy is generally functional herein. The rate of heating, moreover, is also not critical, but it is most practical and preferred to heat as rapidly as possible.

Additional coatings may be applied over these coatings if desired. These can include, for example, SiO_2 coatings, SiO_2/ceramic oxide layers, silicon-containing coatings, silicon-carbon containing coatings, silicon-nitrogen containing coatings, silicon-oxygen-nitrogen coatings, silicon-nitrogen-carbon containing coatings and/or diamond-like carbon coatings. Methods for the application of such coatings are known in the art and many are described in U.S. Patent 4,756,977. An especially preferred coating is silicon carbide applied by CVD of silacyclobutane as is described in U.S. Patent 5,011,706.

After the ceramic layers are applied, the coating covering the bond pads can be etched or partially etched to allow for attachment of leads. The method of etching is not critical and nearly any process known in the art will function herein. This includes, for example, dry etching (eg., with plasma), wet etching (eg., with hydrofluoric acid) and/or laser ablation. If desired, the open bond pads can then be sealed by covering them with one or more non-corroding, conductive layers. The material used for this layer is not critical and can comprise any which is stable in the environment, electrically conductive and useful for interconnecting the circuit. Examples of such materials include gold, copper, silver, tungsten, solder, silver-filled epoxy and the like.

The method for applying this layer or layers is likewise not critical. Examples of such processes include sputtering, electron beam evaporation or by merely dispensing the material at the bond pad. These and other processes are known in the art for use within the multiple layers of the circuit and are functional herein.

It should be noted that the materials of the bond pad (eg., aluminum) are often incompatible with the materials of the non- corroding, conductive layer (eg, gold) such that when they are brought into contact with each other intermetallic formation ("purple plague") can damage the circuit. To prevent such damage, it is within the scope of this invention to first apply a diffusion barrier metal layer to the bond pads followed by application of the conductive layers as set forth above. The diffusion barrier metal layers useful

herein are known in the art for use within integrated circuits for building the multiple layers of the circuit. Generally, such layers comprise metals such as tungsten or metal alloys such as titanium-tungsten, titanium nitride and the like.

The method for forming the diffusion barrier metal layers is not critical and many techniques are known in the art. A common approach involves sputtering the diffusion barrier metal layer on the surface of the circuit followed by etching.

If the bond pads are sealed with this conductive layer, additional ceramic coatings may be added to the above ceramic layers by the methods described above to further seal the circuit.

The above sealing processes can be performed at the wafer stage or after dicing. It is preferred herein, however, to seal the devices at the wafer stage for efficiency reasons.

The integrated circuits formed in the manner of this invention are hermetically sealed such that their reliability is increased. In addition, the circuits can be handled and manipulated without damage. Furthermore, many of the ceramic layers are opaque to UV and visible light.

Such circuits are then interconnected with each other, with a lead frame, with a circuit board or other external components. Such interconnection can be by conventional leads or by methods such as TAB or "flip chip" processes which are well known in the art.

After interconnection, the device can also be packaged by conventional techniques known in the art. For instance, the device can be embedded within an organic encapsulant such as a polyimide, an epoxy or PARYLENE™. It can also be embedded within a silicone encapsulant or it can be included in a plastic package for additional protection.

Claims

1. An integrated circuit having top metallization and one or more bond pads, said circuit characterized by a ceramic layer covering over the integrated circuit, wherein the ceramic layer comprises a silicon-containing ceramic material which is deposited by a process comprising (A) coating the circuit with a composition comprising a preceramic silicon-containing material followed by (B) converting said material to a ceramic and wherein at least a portion of the ceramic layer covering the bond pads has been removed to yield open bond pads for interconnection of the circuit and thereby leaving the ceramic layer in intimate contact with bond pads.

2. The integrated circuit of claim 1 wherein the ceramic layer is selected from the group consisting of silicon oxides, silicon nitride, silicon oxynitride, silicon oxycarbide, silicon carbonitride, silicon oxycarbonitride and silicon carbide.

3. The integrated circuit of claim 1 wherein the preceramic silicon-containing material is hydrogen silsesquioxane resin.

4. The integrated circuit of claim 1 wherein the preceramic silicon-containing material is a hydrolyzed, partially hydrolyzed or their combinations of a formula $R_nSi(OR)_{4-n}$, in which R is an aliphatic, alicyclic or aromatic substituent of 1-20 carbon atoms and n is 0-3.

5. The integrated circuit of claim 1 wherein the ceramic layer is covered by one or more additional ceramic layers selected from SiO_2 coatings, SiO_2/ceramic oxide coatings, silicon coatings, silicon carbon containing coatings, silicon nitrogen containing coatings, silicon oxygen nitrogen containing coatings, silicon carbon nitrogen containing coatings and diamond-like carbon coatings.

6. The integrated circuit of claim 1 wherein the open bond pads are sealed with one or more non-corroding, conductive layers.

7. The integrated circuit of claim 6 wherein the non-corroding, conductive layers comprise a material selected from the group consisting of gold, silver, tungsten, solder, silver filled epoxy and copper.

8. The integrated circuit of claim 1 wherein the open bond pads are sealed with a diffusion barrier metal layer and a non-corroding, conductive layer.

9. The integrated circuit of claim 8 wherein the diffusion barrier metal layer is selected from titanium, an alloy of titanium and tungsten and titanium nitride.

10. The integrated circuit of claim 1 which is interconnected and embedded within a material selected from organic encapsulants and silicone encapsulants.

11. The integrated circuit of claim 1 wherein the ceramic coating is opaque to ultraviolet and visible light.

12. A method for hermetically sealing an integrated circuit having top metallization and one or more bond pads, the method comprising:

    (A) applying a silicon-containing ceramic layer to the integrated circuit by a process which comprises (i) coating the circuit with a composition comprising a preceramic silicon-containing material and followed by (ii) converting

said material to a ceramic; and

(B) removing at least a portion of the silicon-containing ceramic layer covering the bond pads.

13. An integrated circuit comprising:

(A) a circuit subassembly having bond pads;

(B) one or more ceramic layers covering the surface of the subassembly around the bond pads; and

(C) a non-corroding, conductive layer covering the the bond pads;

characterized by one or more of the ceramic layers comprising a silicon-containing ceramic material which is deposited by a process comprising coating at least the primary passivation layer with a composition comprising a preceramic silicon-containing material followed by converting the preceramic material to a ceramic layer.

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-5 136 364 (ROBERT C. BYRNE) * column 1, line 5 - line 24 * * column 1, line 52 - column 2, line 2 * * column 2, line 17 - line 56; figures 1-3 * * column 3, line 14 - line 27; claims 1-3,6,8; figure 5 *	1,2,5-9, 13	H01L21/316 H01L21/56 C04B41/50 H01L23/29 H01L23/31 H01L23/485 C04B41/45
Y		3,4, 10-12	

Y	EP-A-0 427 395 (DOW CORNING CORP.) * column 1, line 1 - line 14 * * column 1, line 28 - column 2, line 28 * * column 2, line 53 - column 4, line 27 * * column 7, line 9 - line 15 *	3,4, 10-12	
A		1,2,5,13	

Y	US-A-4 888 226 (CHING P. WONG) * claim 1; figure *	10	
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X	PROCEEDINGS SPIE - CONF. ON RAPID THERMAL AND INTEGRATED PROCESSING vol. 1595, 10 September 1991, SAN JOSE, CA, USA pages 146 - 164 T.E. GENTLE 'Oxidation of hydrogen silsesquioxane (HSiO3/2)n by rapid thermal processing' * page 146; figure 1 * * page 159 *	1-3,6,7, 11-13	H01L C04B
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	22 DECEMBER 1993	KLOPFENSTEIN P.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	ELECTRONIC PACKAGING AND PRODUCTION vol. 32, no. 2, February 1992, MASSACHUSSETS US page 35 'Packaging ideas: Protective layer eliminates MCM package' * the whole document *	1-3,5,12	
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X	ELECTRONIC PACKAGING MATERIAL SCIENCE SYMPOSIUM 26 November 1990, BOSTON pages 97 - 108 GRISH CHANDRA 'Low temperature ceramic coatings for environmental protection of integrated circuits' * page 97 * * page 100 - page 101; figures 2,3 * * page 104 - page 105; figures 4-7 *	13	
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A	EP-A-0 323 186 (DOW CORNING CORP.) * page 2, line 1 - line 7 * * page 2, line 48 - page 3, line 20 * * page 3, column 33 - column 38 * * page 4, line 1 - line 7 * * page 6, line 20 - line 40 * * page 7, line 27 - line 47 *	1-3,5, 11-13	TECHNICAL FIELDS SEARCHED (Int. Cl.5)

A	DE-A-3 805 490 (MITSUBISHI DENKI K.K.) * column 3, line 66 - column 4, line 56; figure 3 * * column 5, line 32 - line 45; claims 1,4,6-8 *	1,2,4, 10-13	

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L : document cited for other reasons

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